

AA55K-M1S REV 7.1**Model Name:A55MLC2****2012/05/25**

CPU: AMD FM1

System

Chipset: HUDSON-D2 A55

Main

Memory: Dual Channel/DDR-III*2(Max 16GB) 800/1066/1333/1600/1866

Onboard Device:

Super I/O:IT8772E

LAN : RTL8105EL

HD Codec:ALC662 3 jacks

Power solution:

CPU Voltage Regulators:3phase by ISL6328

VDDNB voltage Regulators:1phase by ISL6328

APU_VDDR/P_RUN voltage Regulators:LDO

DDR voltage Regulators:1Phase by UPI1514

Expansion Slots:

PCI EXPRESS 16X SLOT*1

PCI EXPRESS 1X SLOT*1

REAR I/O:

PS/2 KBMS*1

VGA Port*1

2 layer USB2.0 (2.0)*1

2 layer USB2.0 (2.0)+ RJ45 Ports*1

Audio Jackets 3jets*1

Front I/O:

SATA2 Connectors*4

USB2.0 Header*2

CPU FAN*1

System1 FAN*1

Serial header*1

Front Audio Header*1

Front Panel Header*1

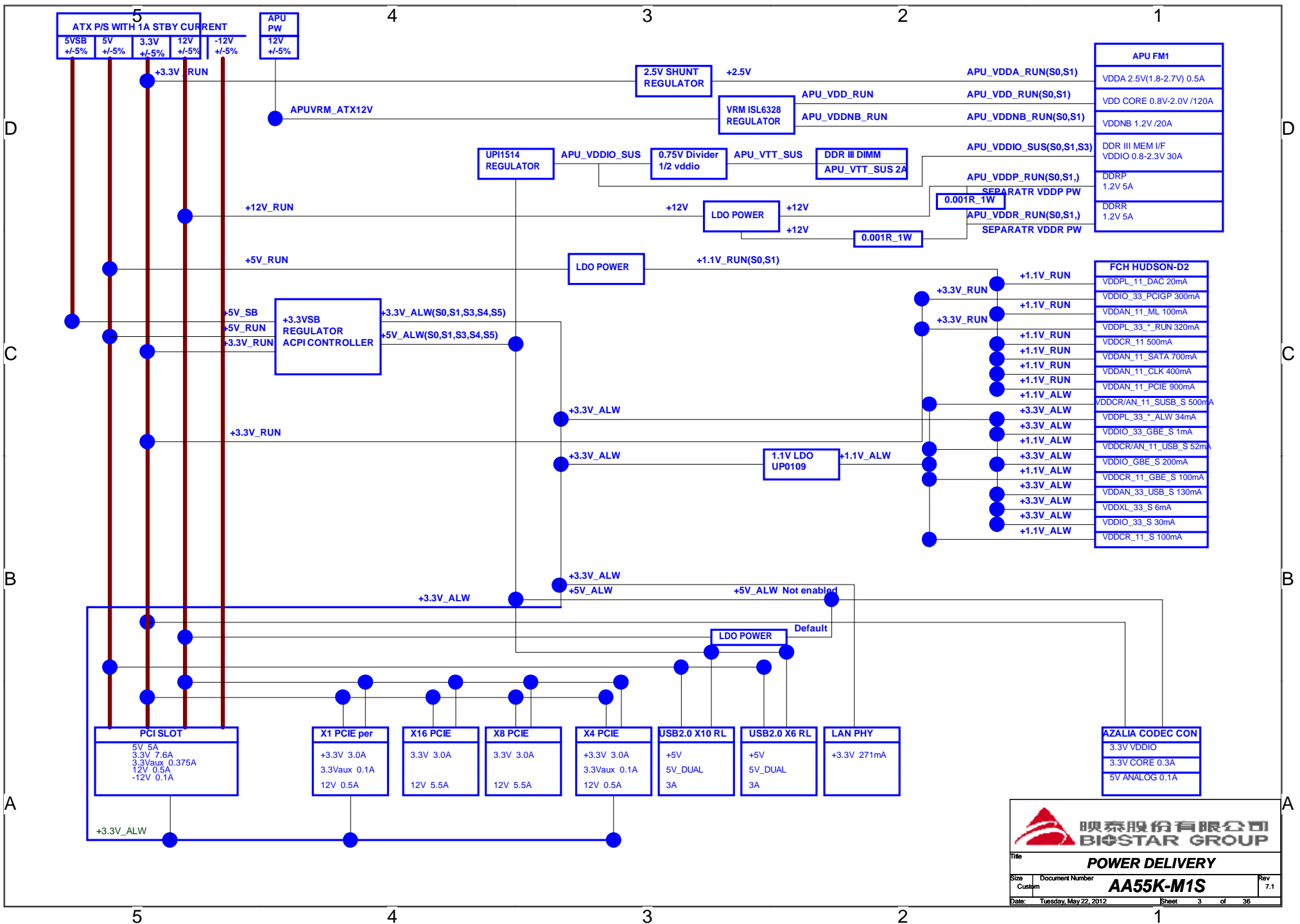
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22	USB CONN
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24	AUDIO CONNECTOR
25	SUPER I/O ITE8772E
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30	FRONT USB
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32	VCC_CORE-ISL6328
33	MEMORY POWER/EUP
34	APU VDDPR/FCH POWER
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36	BOM

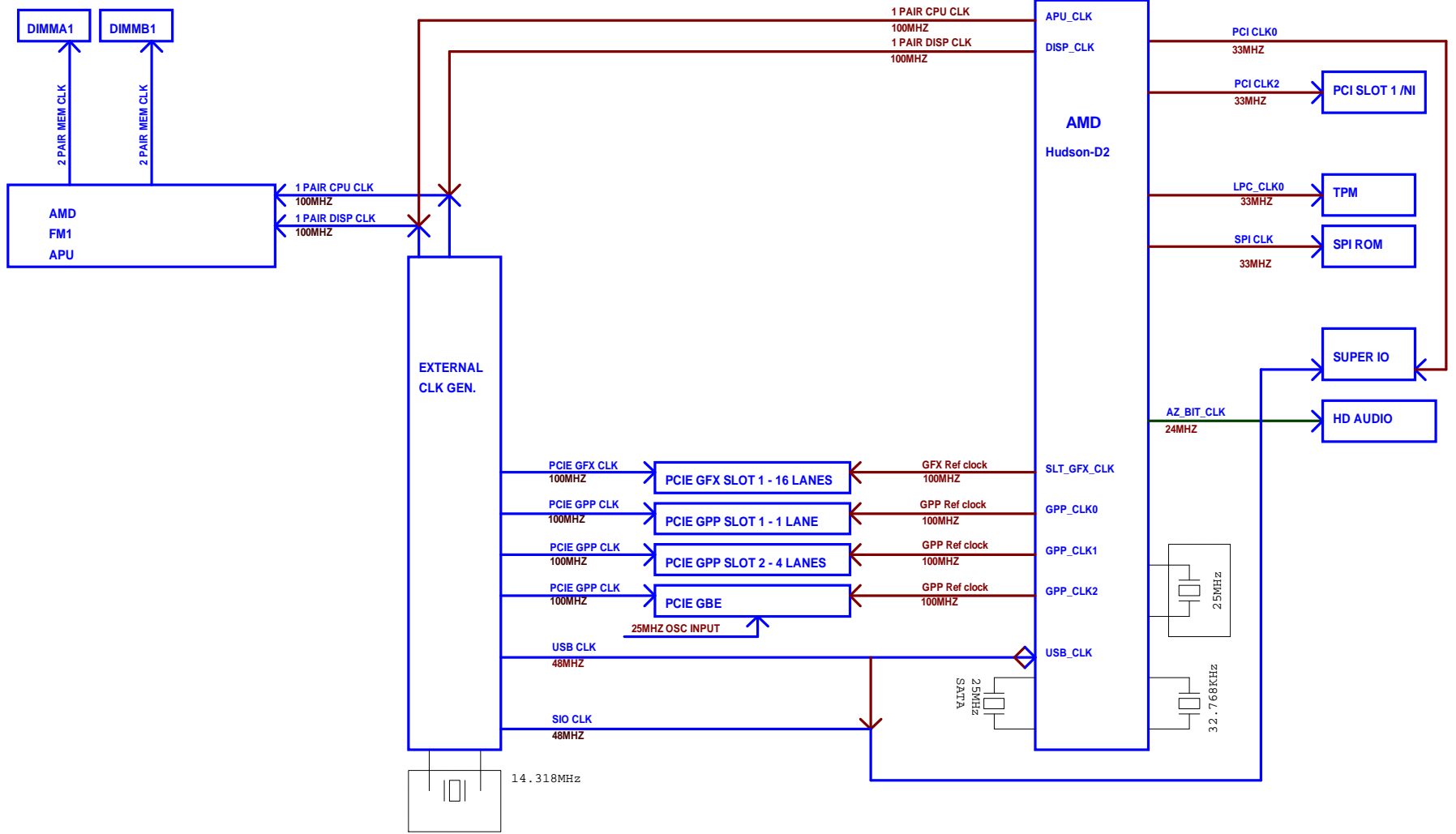
HW Engineer:**Date:****HW Leader1:****Date:**

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 映泰股份有限公司 BIOSTAR GROUP COVER	
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External clock mode

Internal clock mode



映泰股份有限公司
BIOSAR GROUP

Title CLOCK DISTRIBUTION			Rev 7.1
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- 1.Change FCH to A13 B3 version
2.Colay Lan Chip RTL8111F to VER 7.1

D

C

B

A

 映泰股份有限公司 BIOSTAR GROUP		
Title REVISION HISTORY		
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5

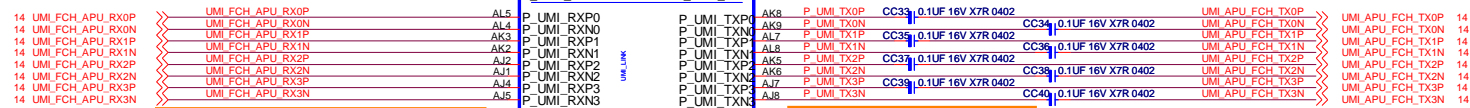
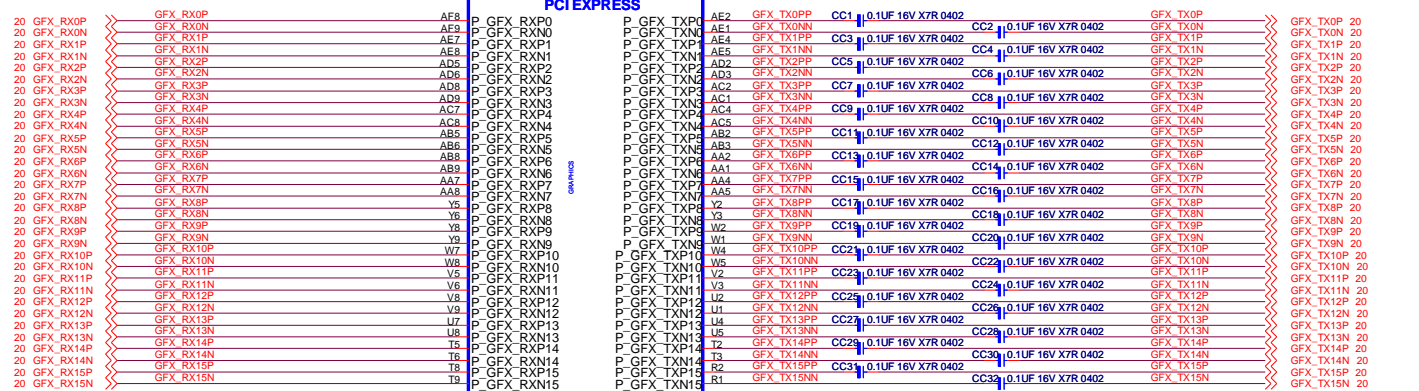
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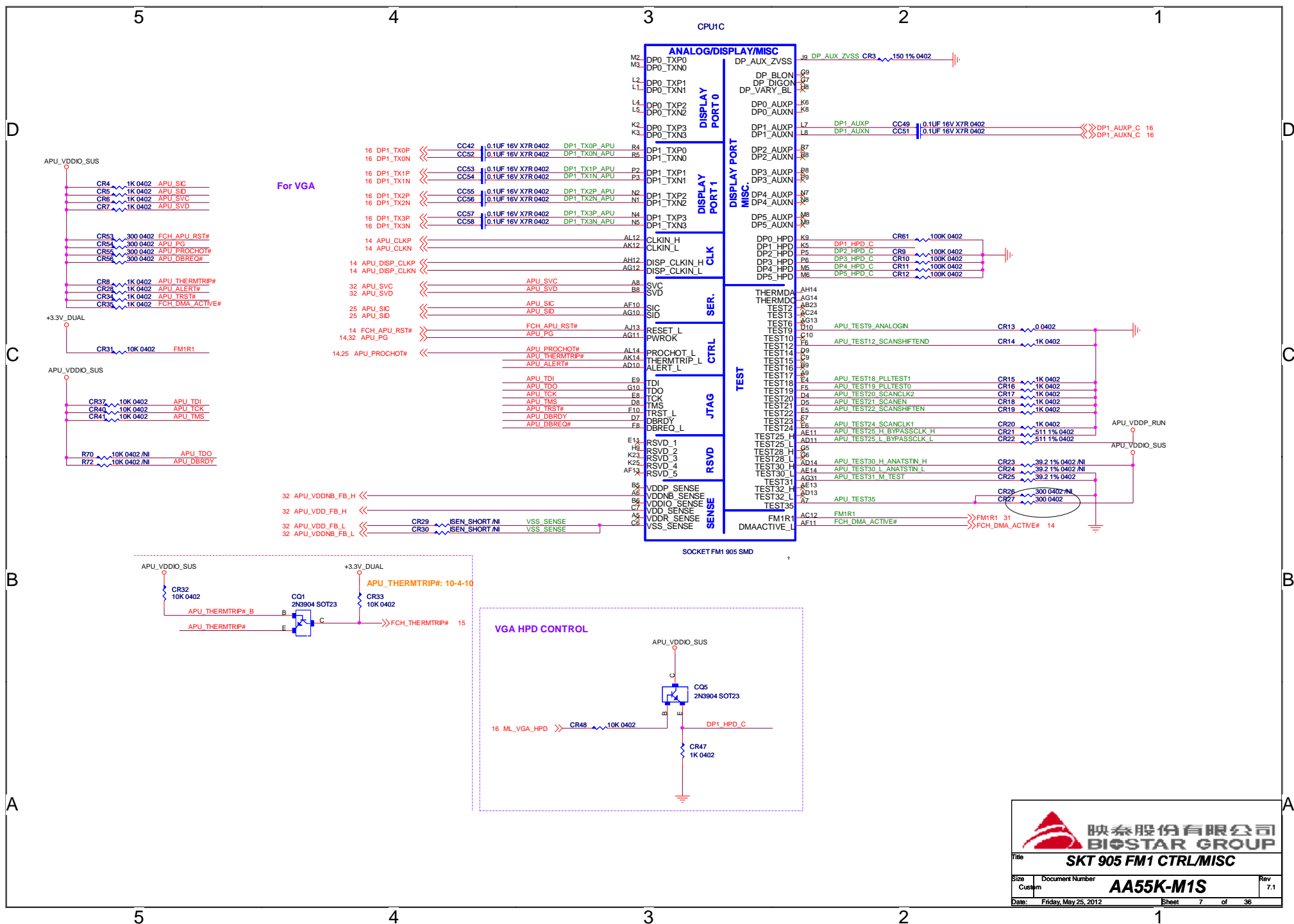
CPU1H

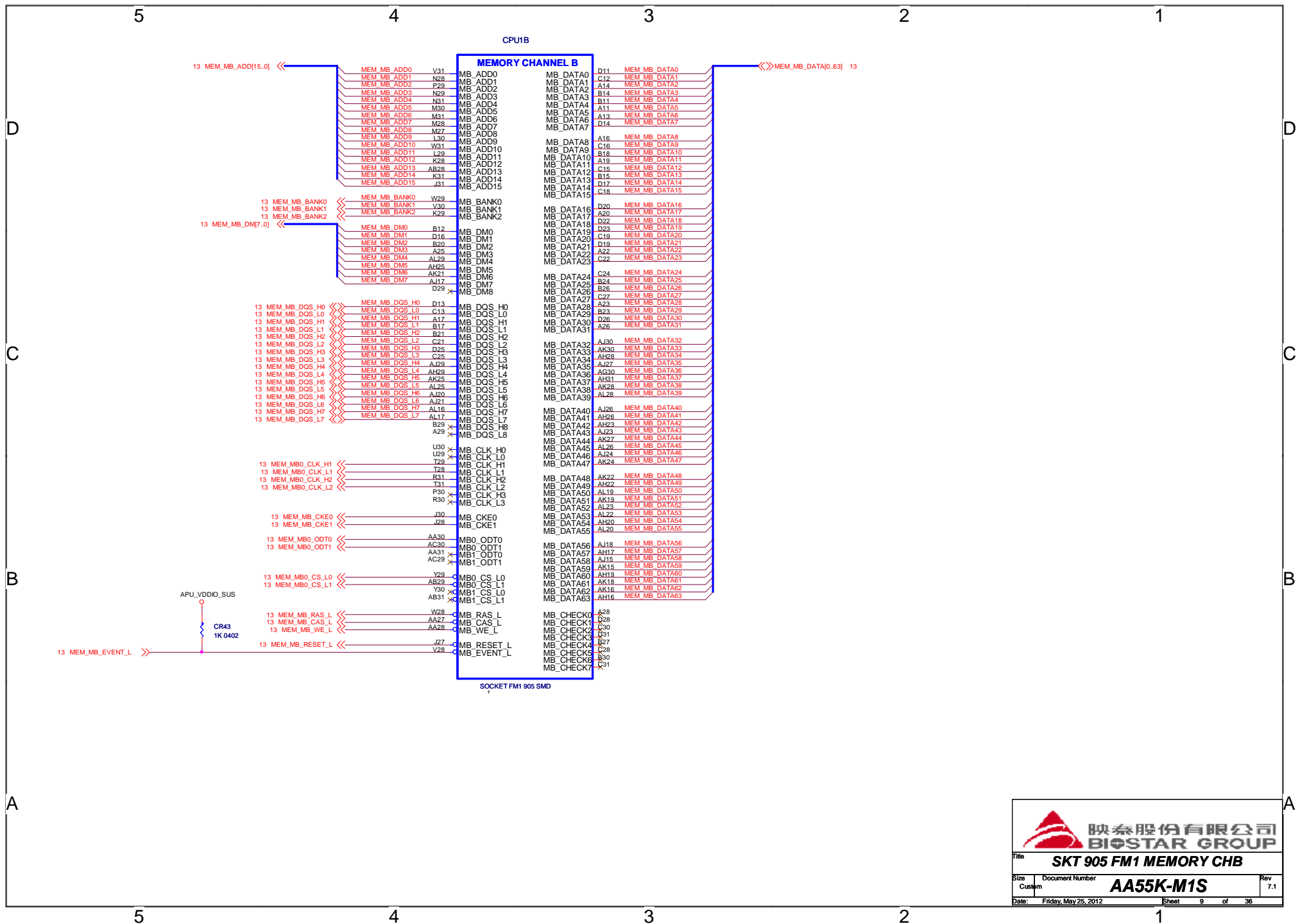
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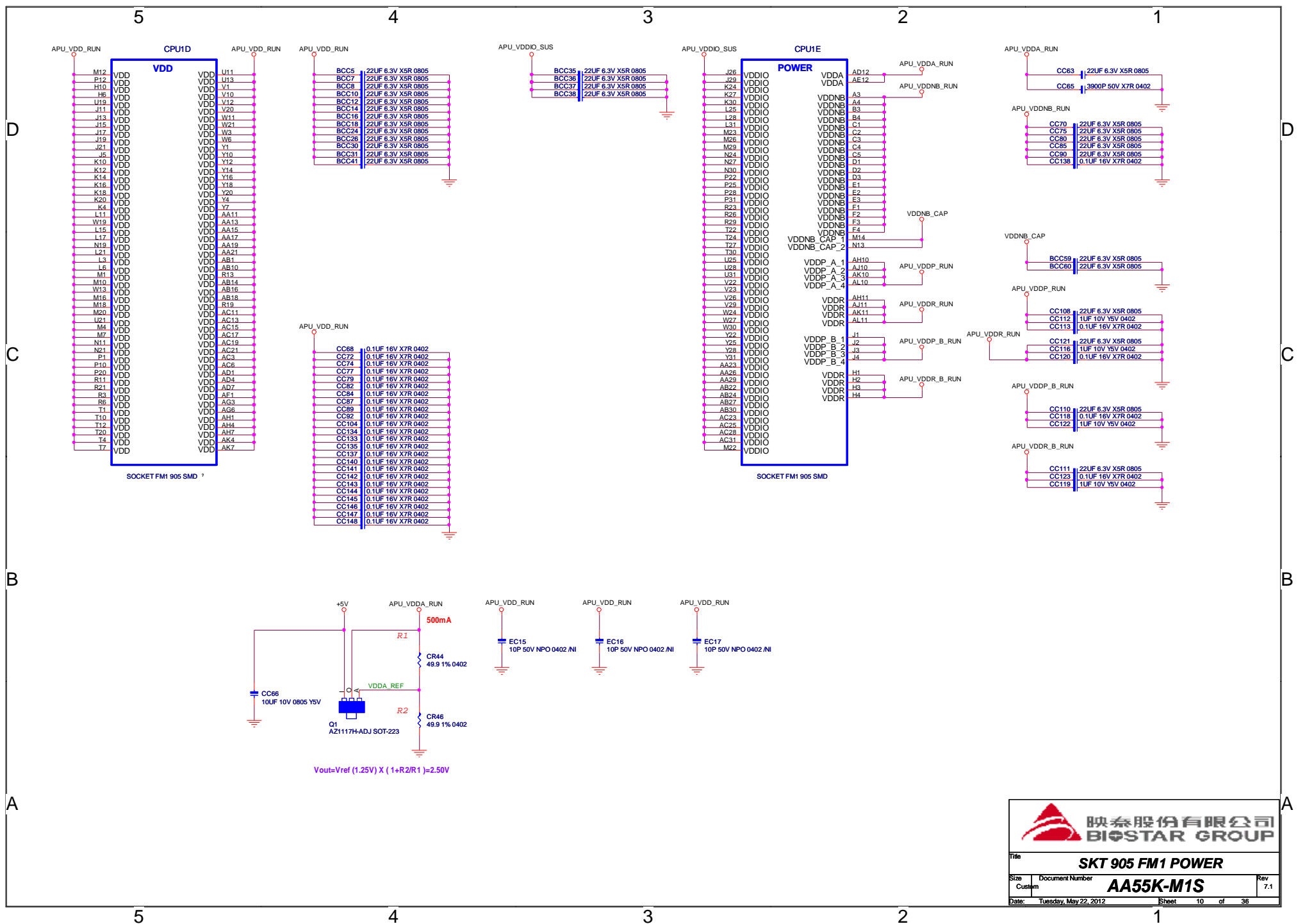
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1









5

4

3

2

1

CPU1F

CPU1G

A10	VSS	1	VSS	59	G30
A12	VSS	2	VSS	60	G4
A15	VSS	3	VSS	61	H5
A18	VSS	4	VSS	62	H13
A21	VSS	5	VSS	63	H16
A24	VSS	6	VSS	64	H19
A27	VSS	7	VSS	65	H2
A9	VSS	8	VSS	66	H25
B10	VSS	9	VSS	67	H28
B13	VSS	10	VSS	68	H31
B16	VSS	11	VSS	69	H5
B19	VSS	12	VSS	70	H7
B22	VSS	13	VSS	71	J10
B25	VSS	14	VSS	72	J12
B28	VSS	15	VSS	73	J14
B7	VSS	16	VSS	74	J16
C11	VSS	17	VSS	75	J18
C14	VSS	18	VSS	76	J20
C17	VSS	19	VSS	77	J22
C20	VSS	20	VSS	78	J23
C23	VSS	21	VSS	79	J8
C26	VSS	22	VSS	80	K1
C29	VSS	23	VSS	81	K11
C8	VSS	24	VSS	82	V13
D12	VSS	25	VSS	83	K15
D15	VSS	26	VSS	84	K17
D18	VSS	27	VSS	85	V19
D21	VSS	28	VSS	86	K21
D24	VSS	29	VSS	87	K7
D27	VSS	30	VSS	88	L10
D30	VSS	31	VSS	89	L12
D6	VSS	32	VSS	90	L14
E10	VSS	33	VSS	91	L16
E13	VSS	34	VSS	92	L18
E16	VSS	35	VSS	93	L20
E19	VSS	36	VSS	94	L22
E22	VSS	37	VSS	95	L2
E25	VSS	38	VSS	96	M11
E28	VSS	39	VSS	97	M13
E31	VSS	40	VSS	98	M15
E7	VSS	41	VSS	99	M17
F11	VSS	42	VSS	100	M21
F14	VSS	43	VSS	101	N10
F17	VSS	44	VSS	102	N12
F20	VSS	45	VSS	103	N20
F23	VSS	46	VSS	104	N22
F26	VSS	47	VSS	105	N3
F29	VSS	48	VSS	106	N6
F9	VSS	49	VSS	107	N9
G1	VSS	50	VSS	108	P11
G12	VSS	51	VSS	109	P21
G15	VSS	52	VSS	110	P4
G18	VSS	53	VSS	111	P7
G2	VSS	54	VSS	112	R10
G21	VSS	55	VSS	113	R12
G24	VSS	56	VSS	114	R20
G27	VSS	57	VSS	115	R22
G3	VSS	58	VSS	116	R9

SOCKET FM1 905 SMD

T11	VSS	AE3
T21	VSS	AE30
U10	VSS	AE6
U12	VSS	AE9
U20	VSS	AF12
U22	VSS	AF14
U3	VSS	AF16
U6	VSS	AF19
U9	VSS	AF22
V11	VSS	AF25
V21	VSS	AF28
V4	VSS	AF31
V7	VSS	AF4
W10	VSS	AF7
W12	VSS	AG17
W20	VSS	AG20
W22	VSS	AG23
W9	VSS	AG26
Y11	VSS	AG29
Y13	VSS	AG9
Y15	VSS	AH13
Y17	VSS	AH15
Y19	VSS	AH18
Y21	VSS	AH21
AA10	VSS	AH24
AA14	VSS	AH27
AA18	VSS	AH30
AA22	VSS	AJ12
AA3	VSS	AJ14
AA6	VSS	AJ16
AA9	VSS	AJ19
AB11	VSS	AJ22
AB13	VSS	AJ25
AB15	VSS	AJ28
AB17	VSS	AJ3
AB19	VSS	AJ31
AB21	VSS	AJ6
AB4	VSS	AJ8
AB7	VSS	AK13
AC10	VSS	AK17
AC14	VSS	AK20
AC16	VSS	AK23
AC18	VSS	AK26
AC20	VSS	AK29
AC22	VSS	AL13
AC9	VSS	AL15
AD17	VSS	AL18
AD20	VSS	AL21
AD23	VSS	AL24
AD26	VSS	AL27
AD29	VSS	AL3
AE10	VSS	AL6
AE15	VSS	M19
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AE21	VSS	P19
AE24	VSS	T13
AE27	VSS	T19

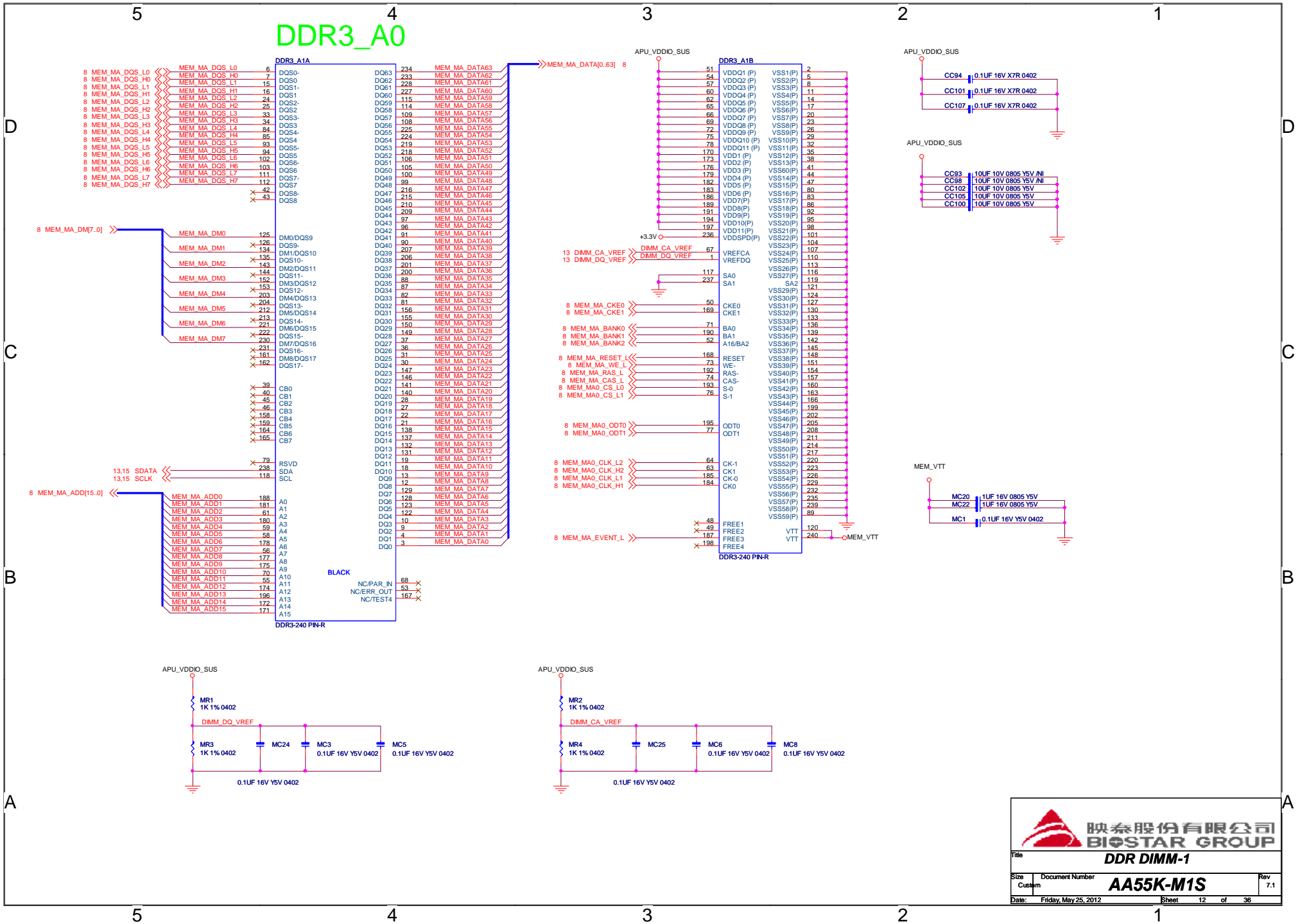
SOCKET FM1 905 SMD

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NO:2011_AMD_FM1_01

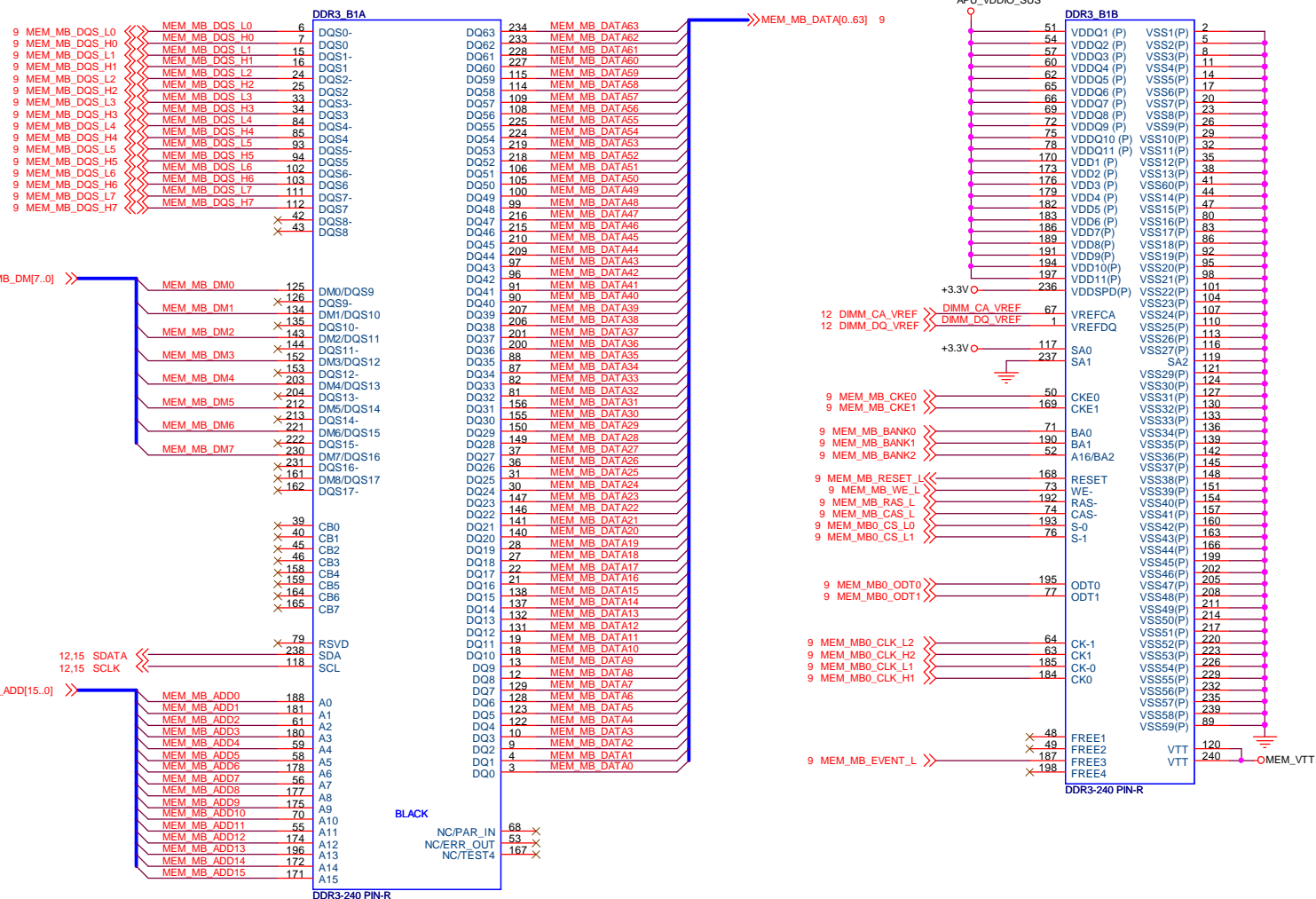


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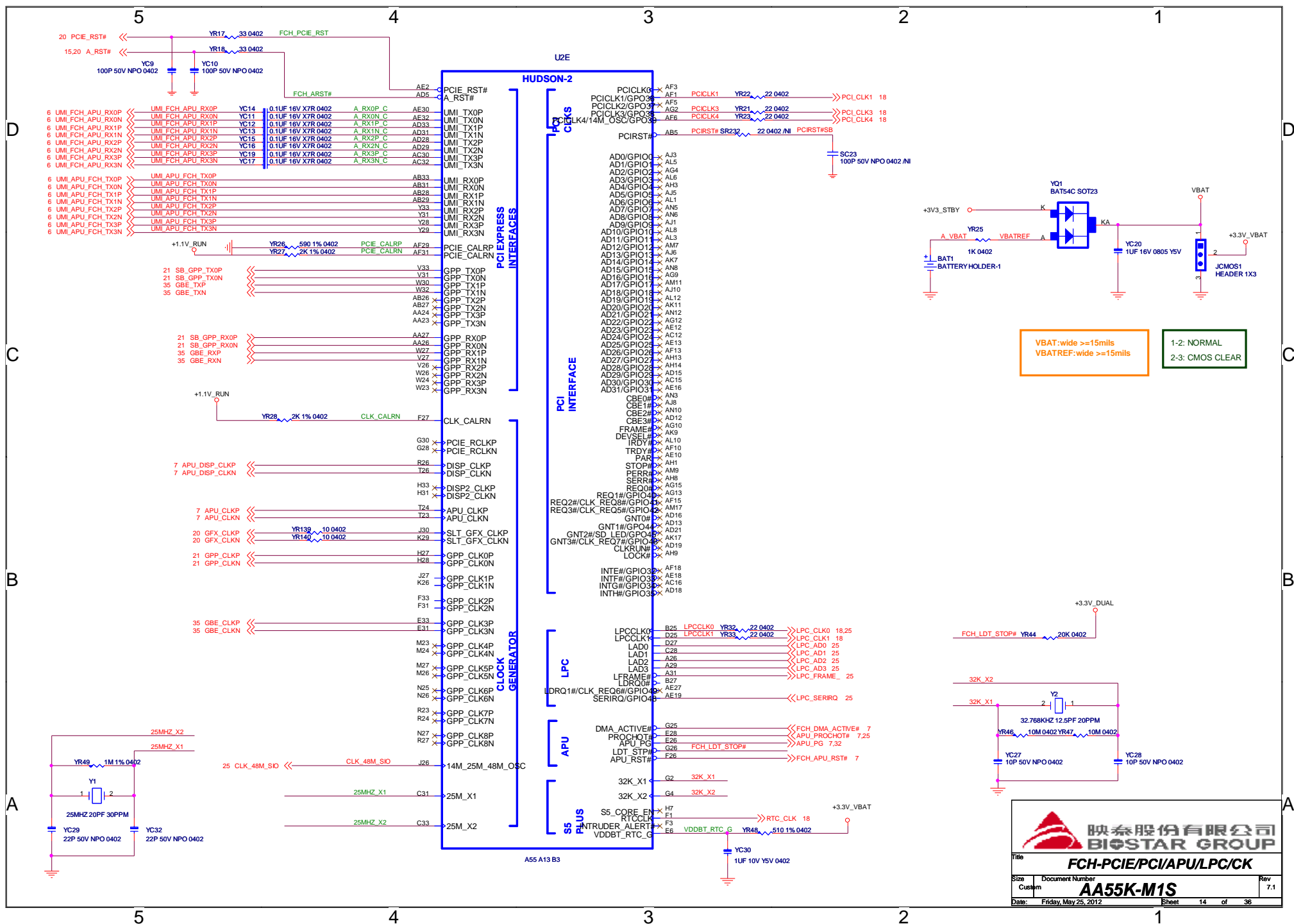
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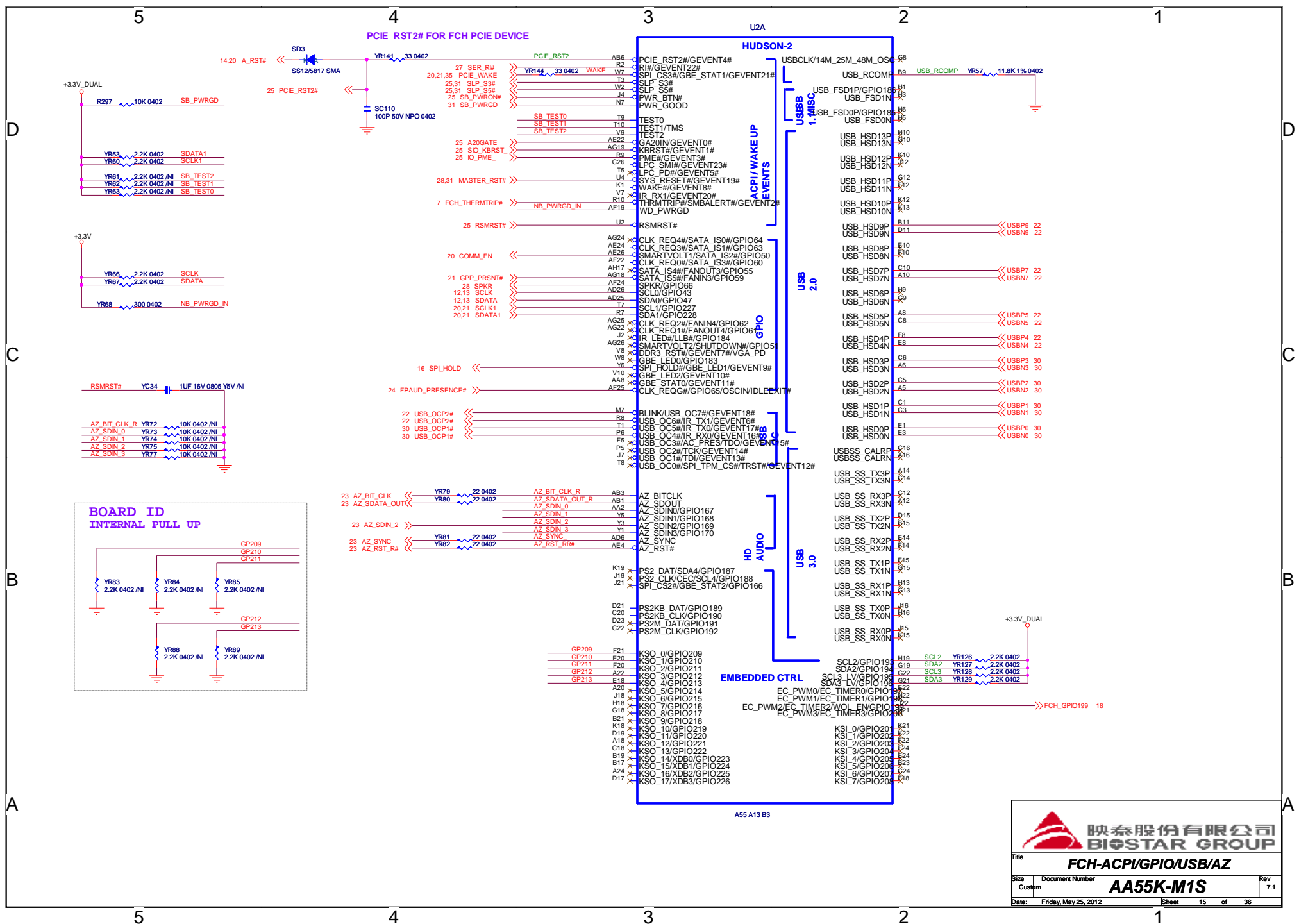


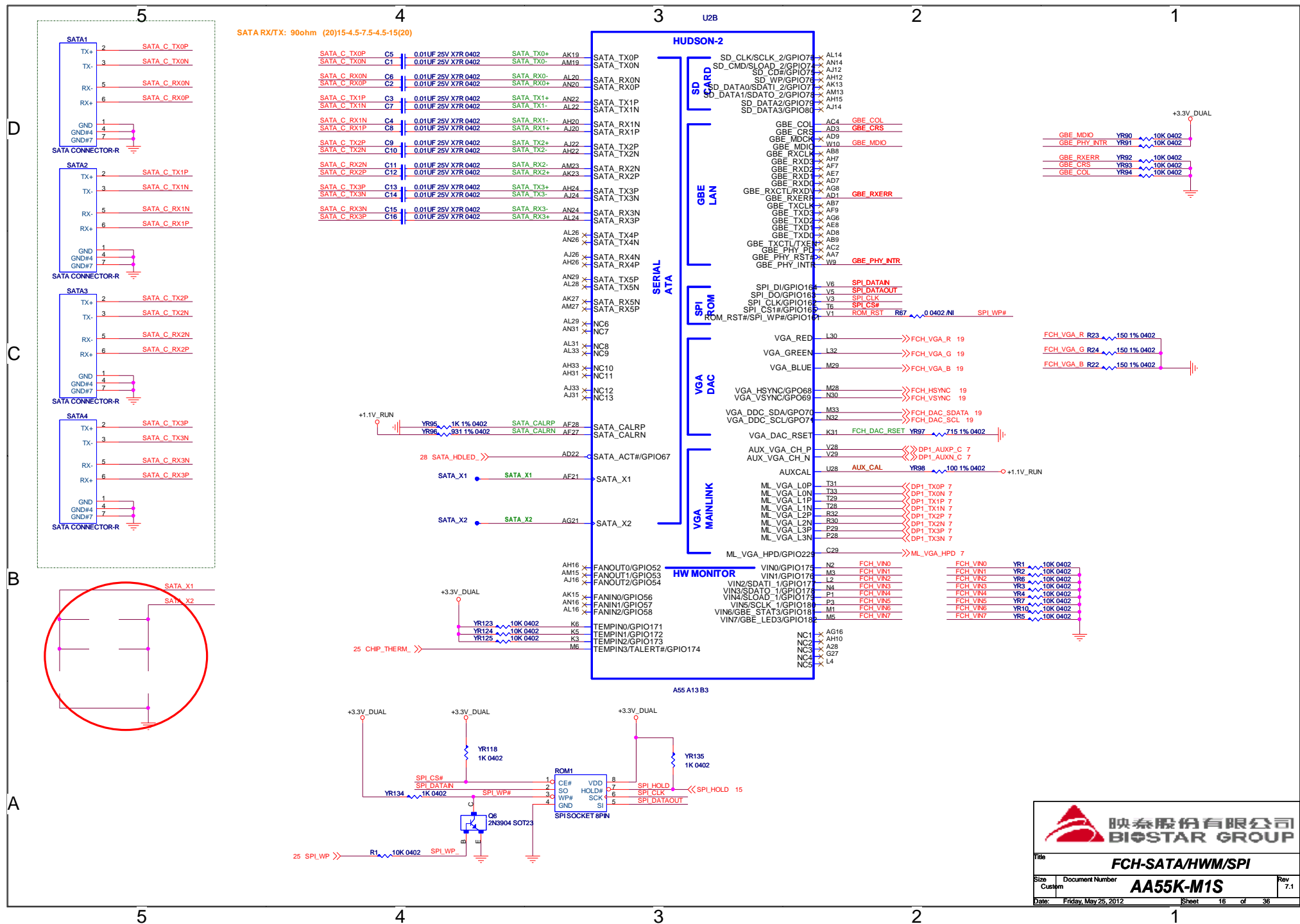
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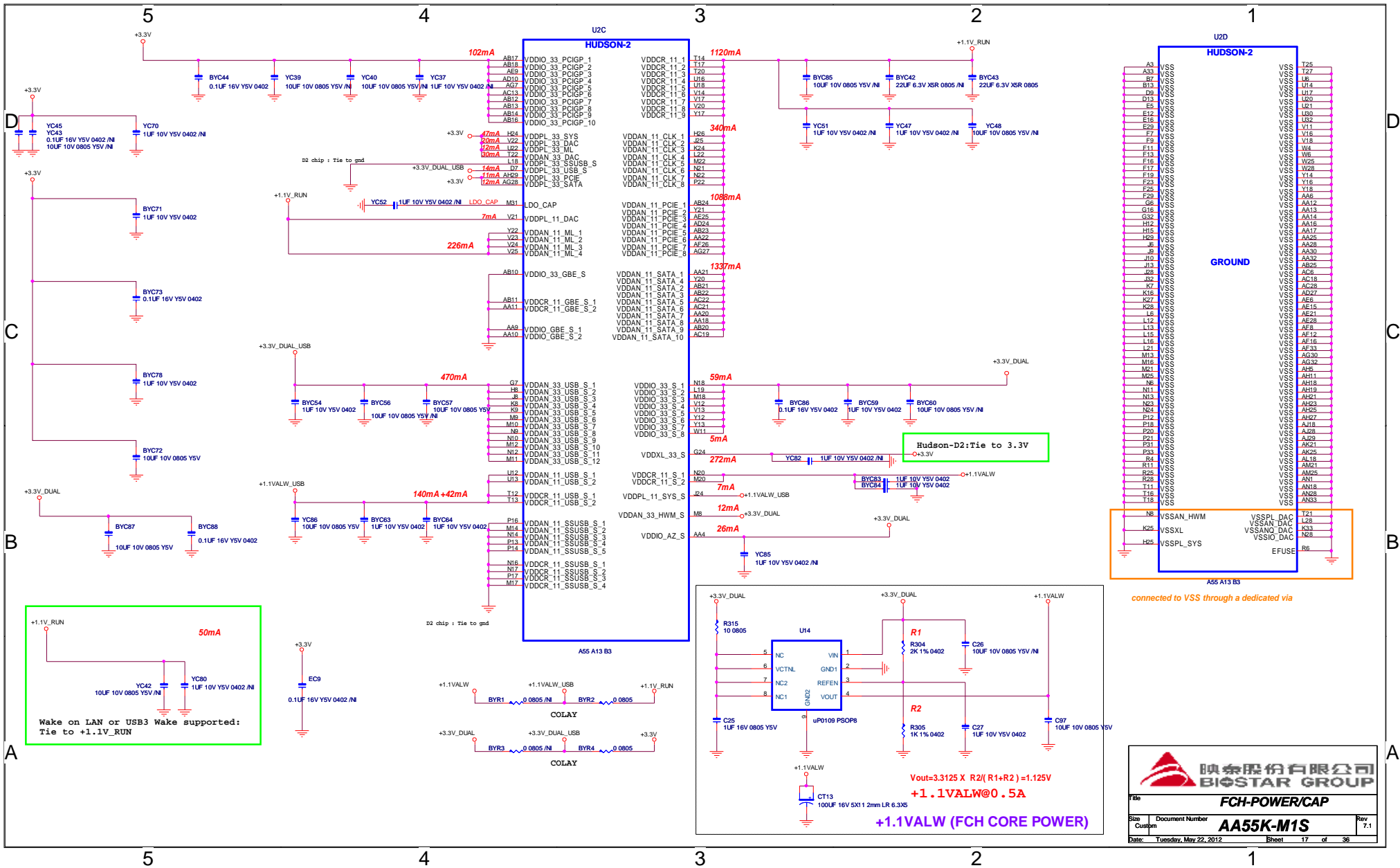


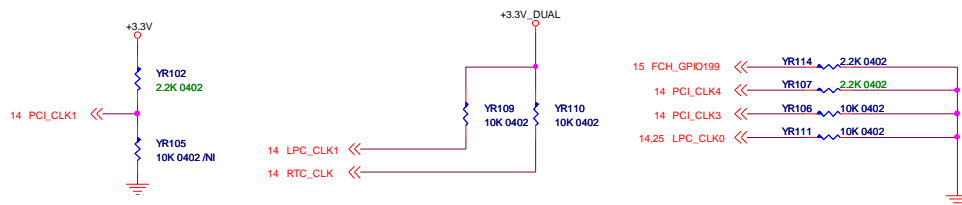
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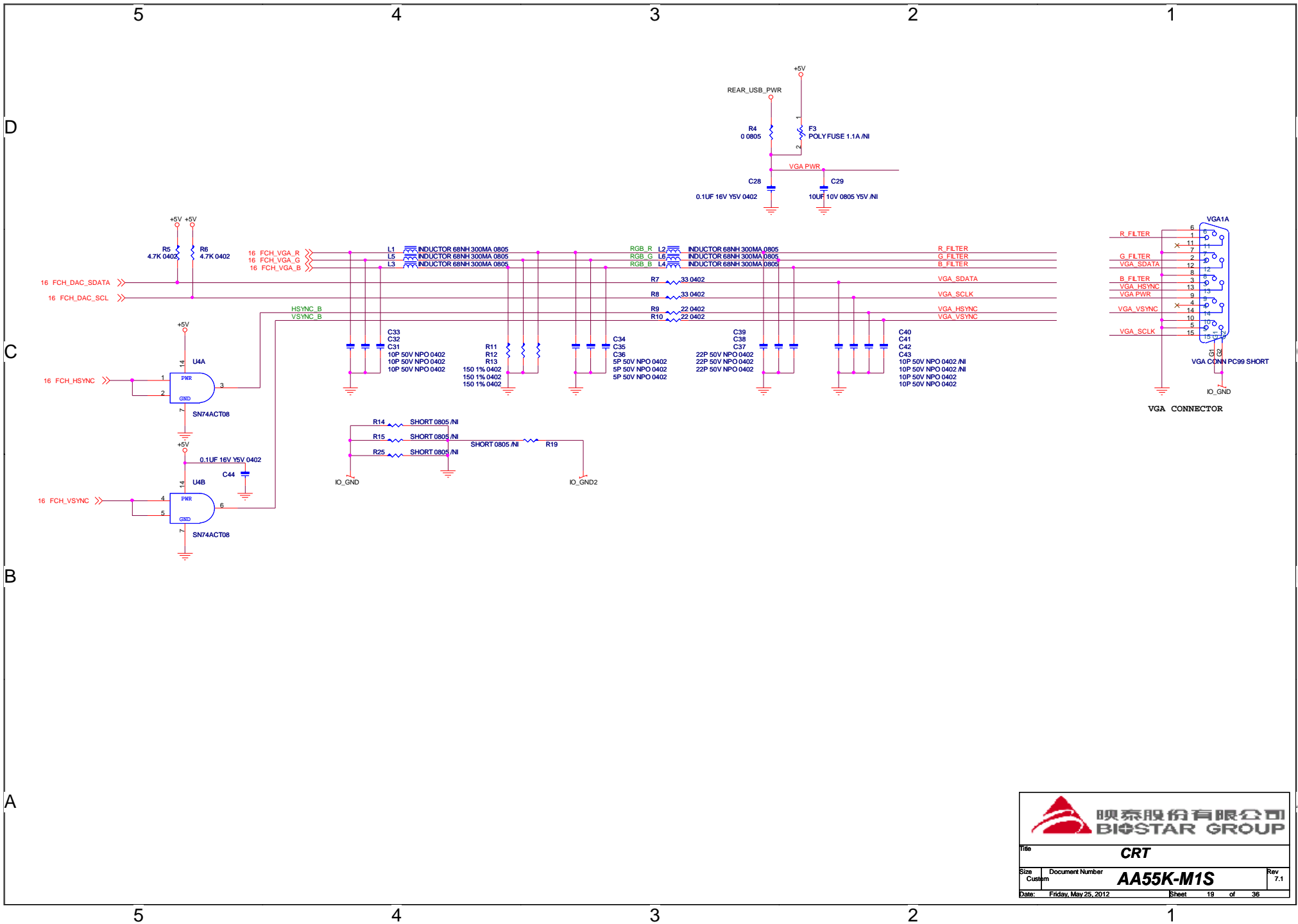


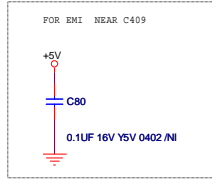
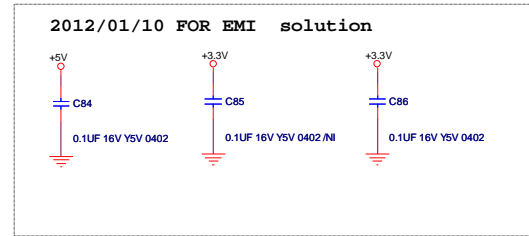
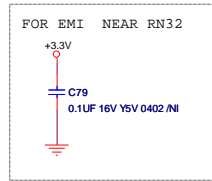
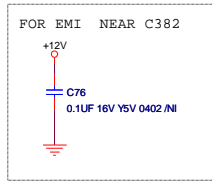
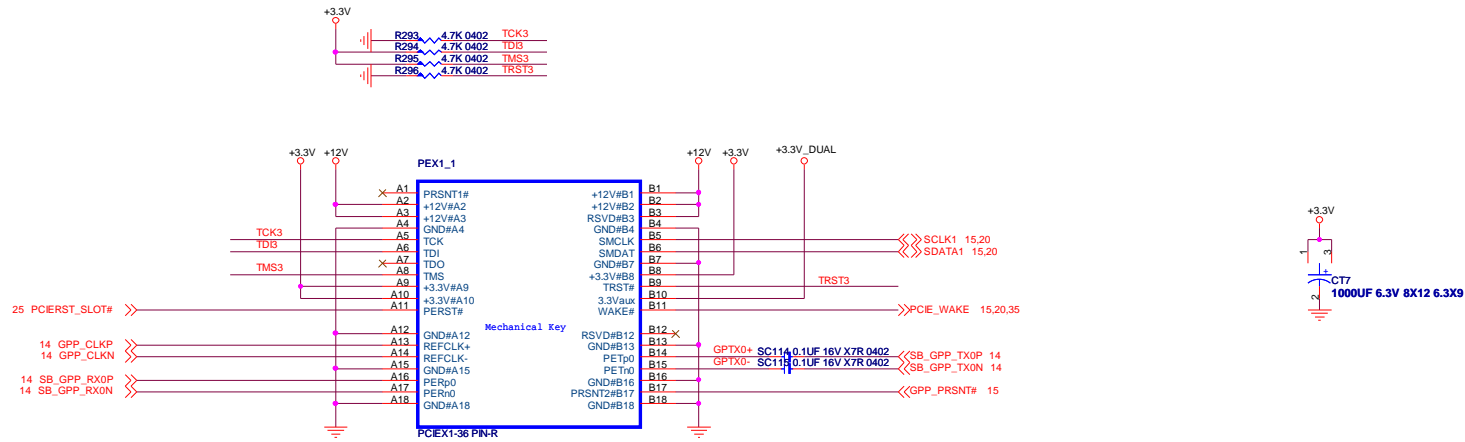


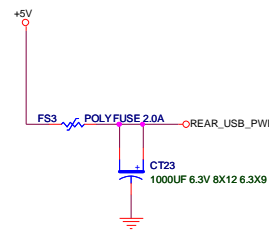
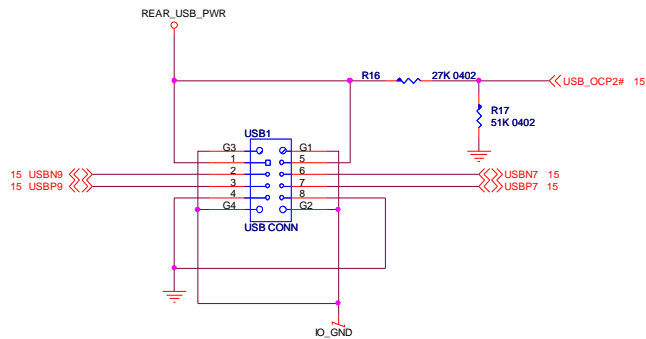
REQUIRED STRAPS

	RTC_CLK	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO199
PULL HIGH	SS+ DISABLE DEFAULT	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	NON-FUSION CPU CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	ROM TYPE: H=LPC ROM
PULL LOW	SS+ ENABLE	FORCE PCIE GEN1	IGNORE DEBUG STRAPS DEFAULT	FUSION CPU CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED	L = SPI ROM DEFAULT

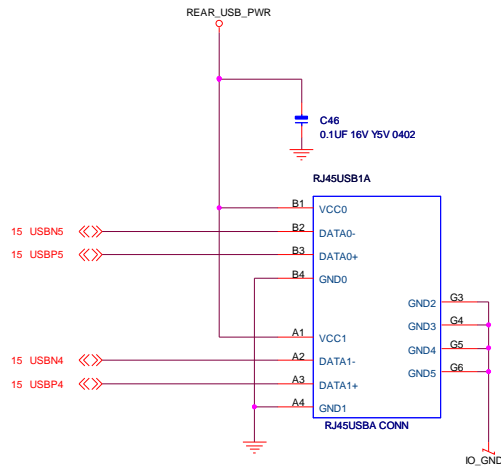
NOTE: HUDSON-D1 HAS INTERNAL 15K PULL UP RESISTOR FOR PCI_AD[30:23]



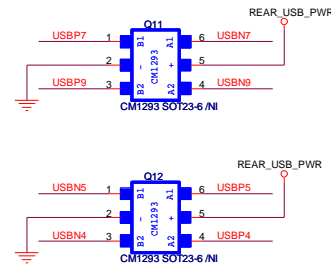




REAR USB POWER



REAR USB



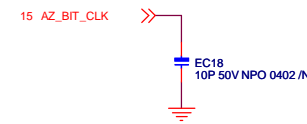
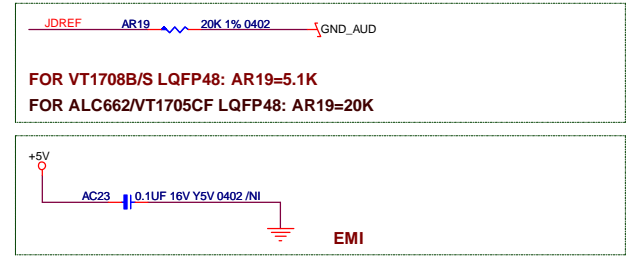
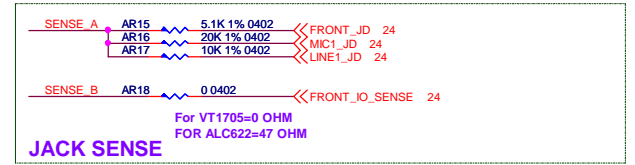
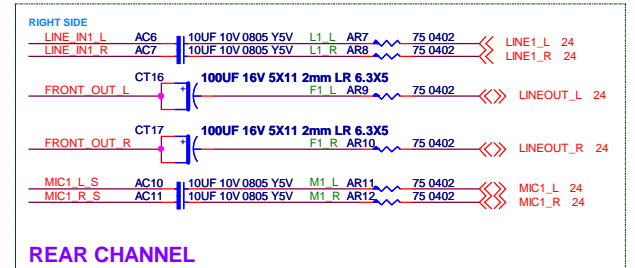
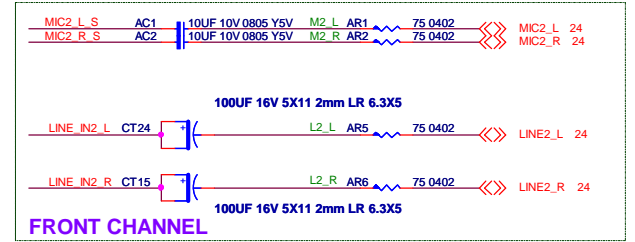
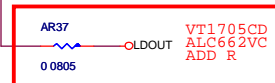
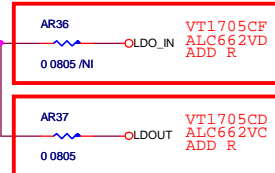
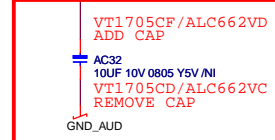
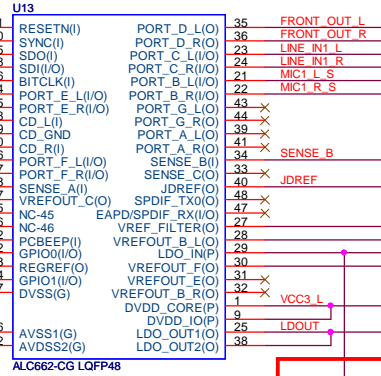
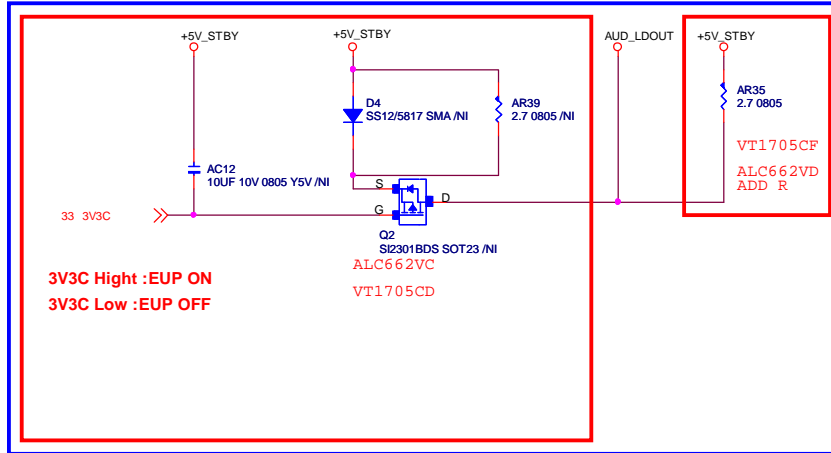
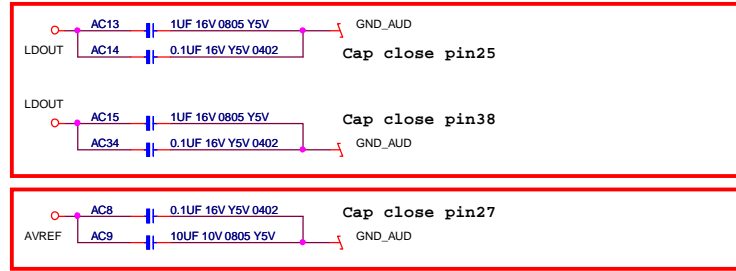
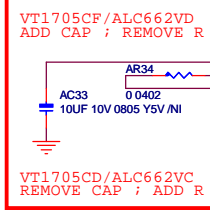
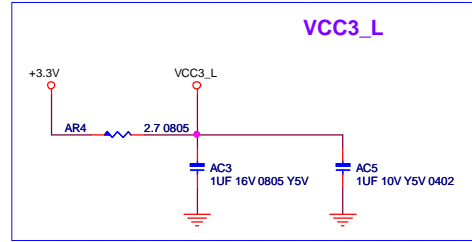
REAR USB ESD



AMD Motherboard Design Guide 1.6 update

AUDIO PART: A+Reference

15 AZ_RST_R#
15 AZ_SYNC
15 AZ_SDAT_A_OUT
15 AZ_SDIN_2
15 AZ_BIT_CLK



Title

ALC662VC/VT1705CF

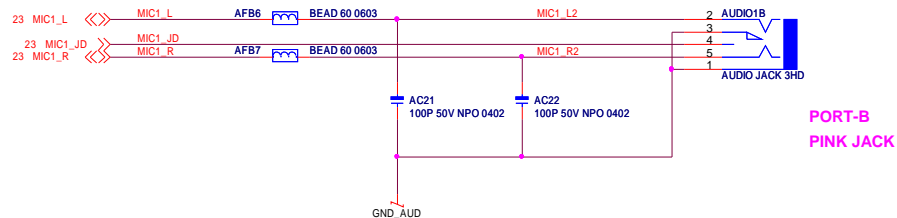
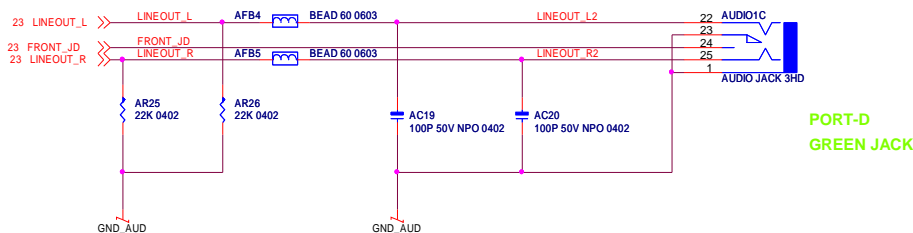
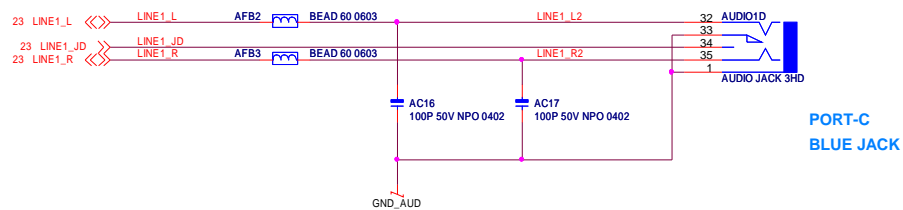
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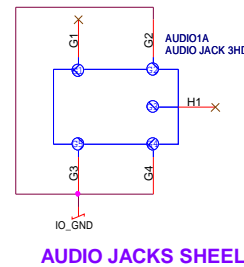
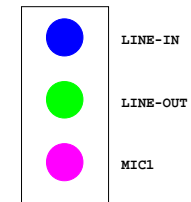
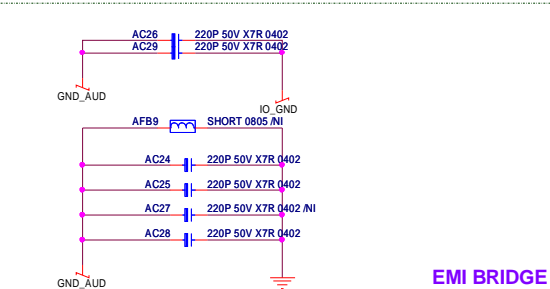
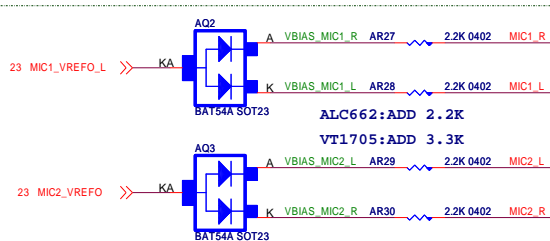
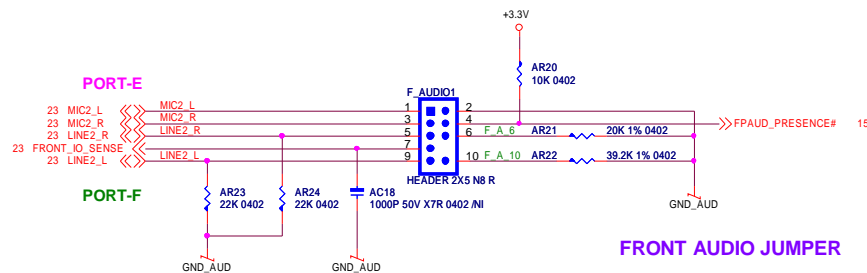
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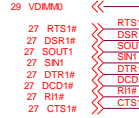
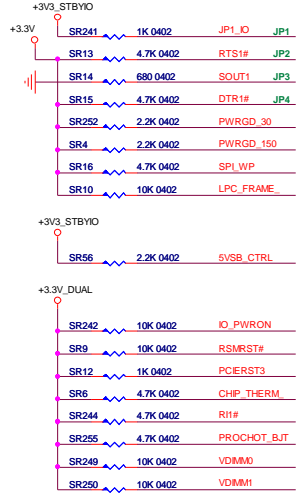


REAR AUDIO JACKS

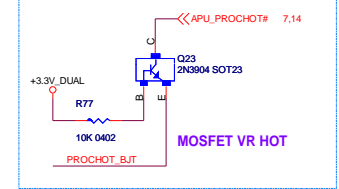
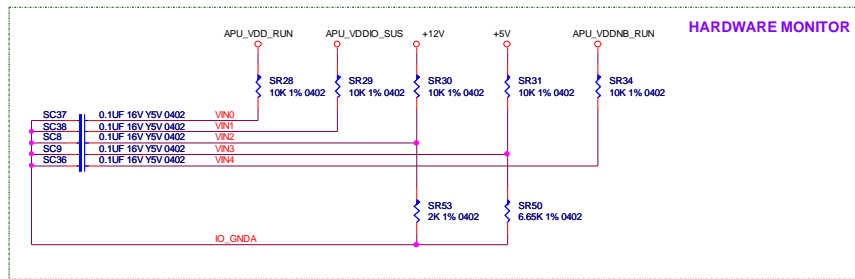
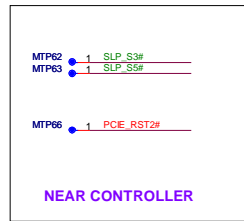
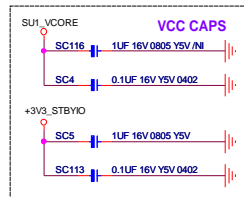
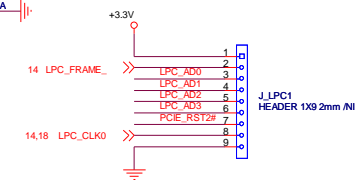
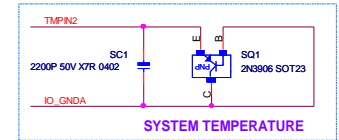
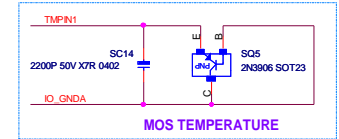
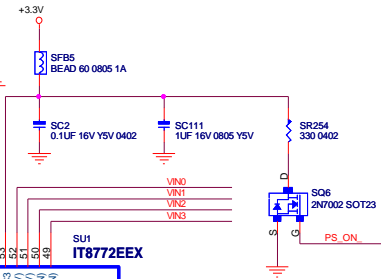
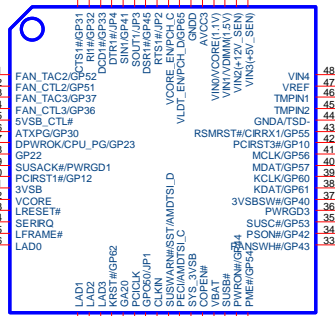


Power-On Strapping

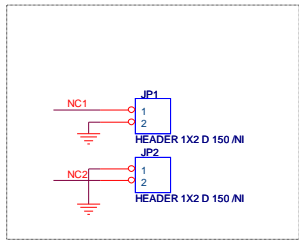
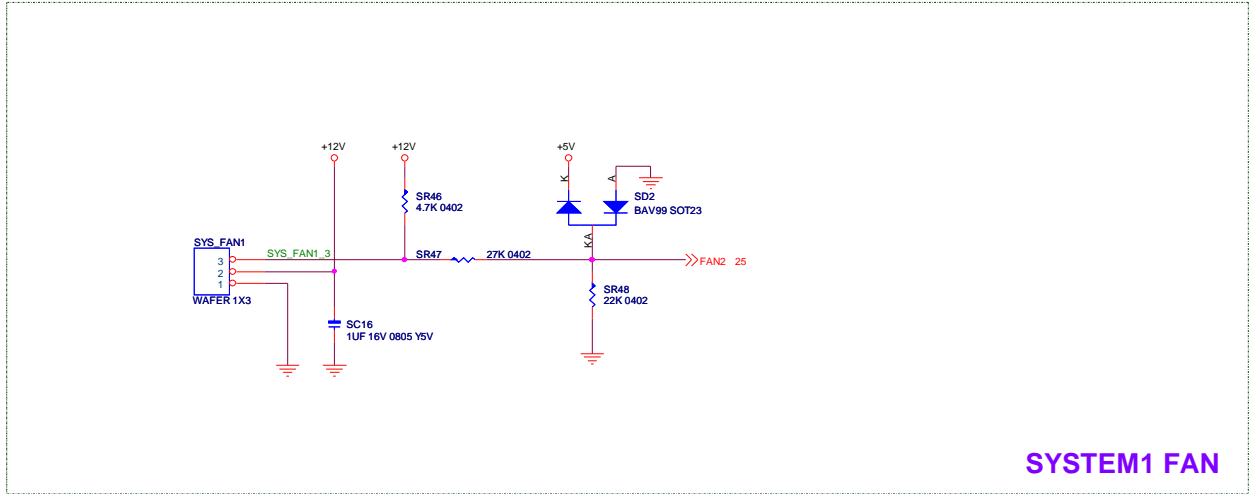
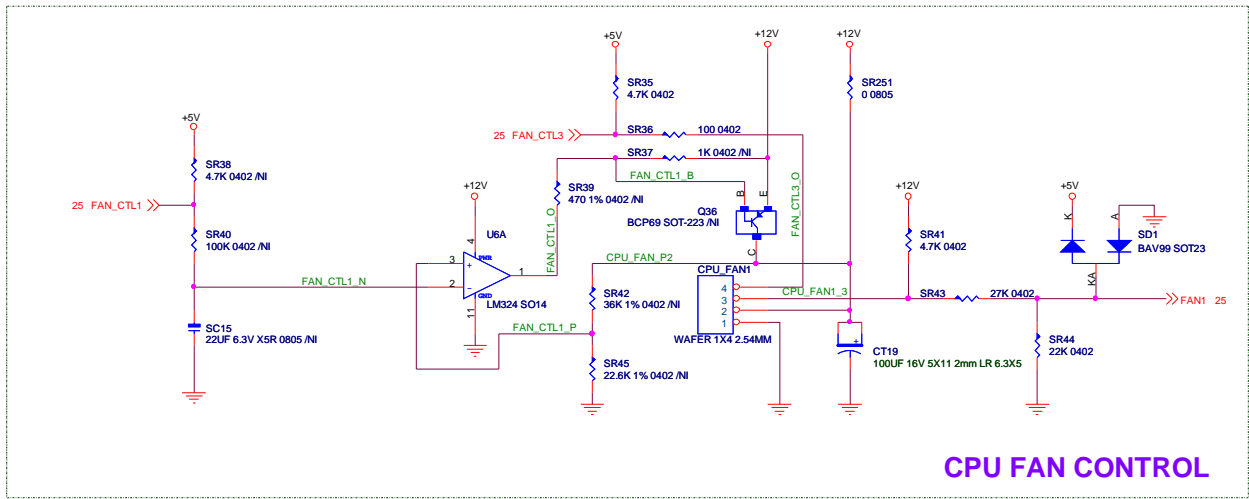
	Symbol	Value	Description
JP1	DSW_EUP_SEL	1	EUP(default)
Pin-23	DSW	0	DSW
JP2	WDT_EN	1	Disable WDT to reset PWROK(default)
Pin-57	WDT	0	Enable WDT to reset PWROK
JP3	FAN_CTL_SEL	1	EC Index 6Bh/73h default = 80h(Fan off)
Pin-59	FAN	0	EC Index 6Bh/73h default = 00h(Full speed)
JP4	K8PWR_EN	1	Disable K8 Power Sequence(default)
Pin-61	K8PWR	0	Enable K8 Power Sequence



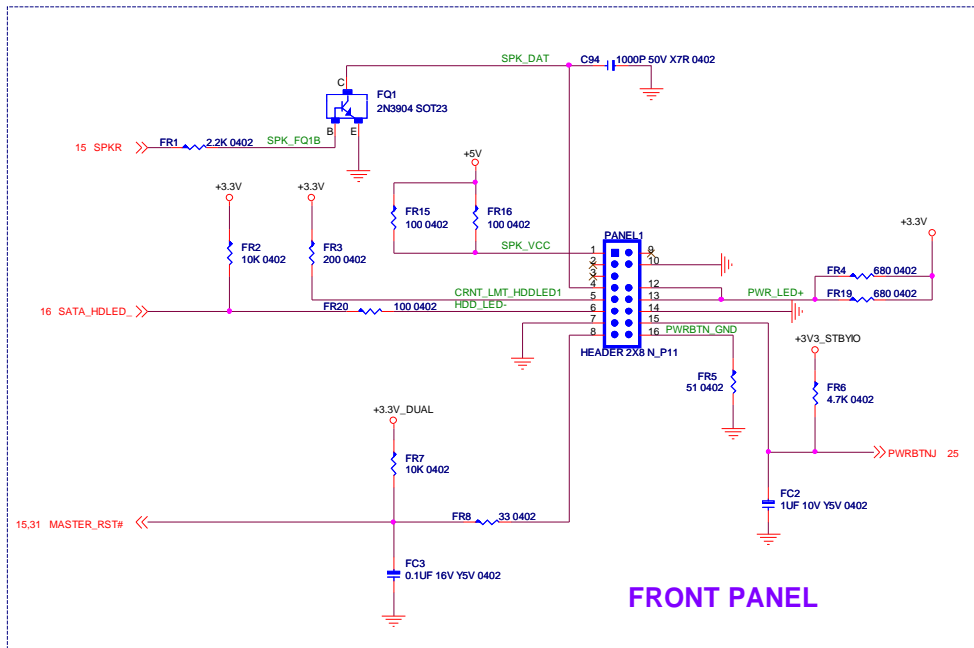
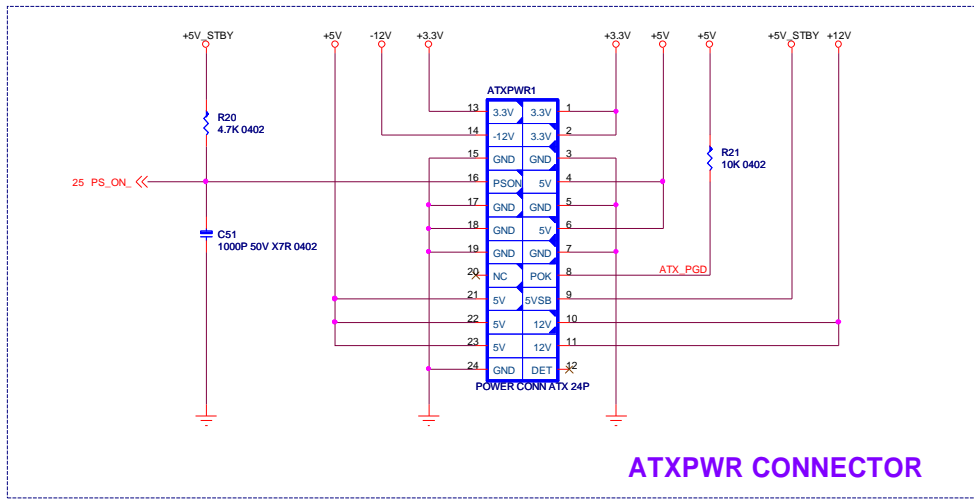
64-IQFP

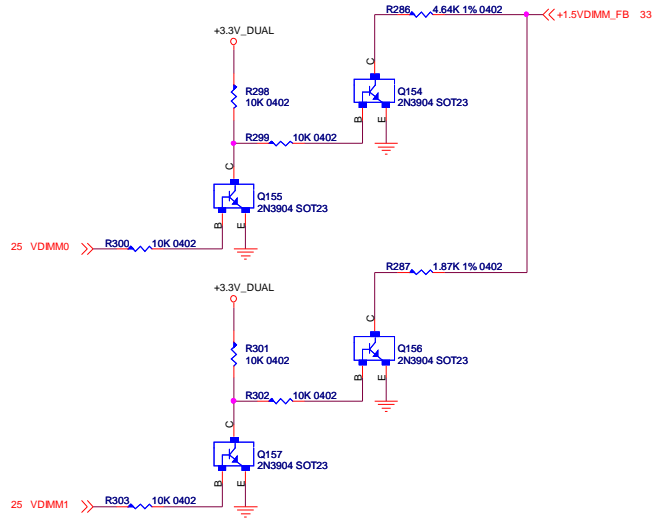


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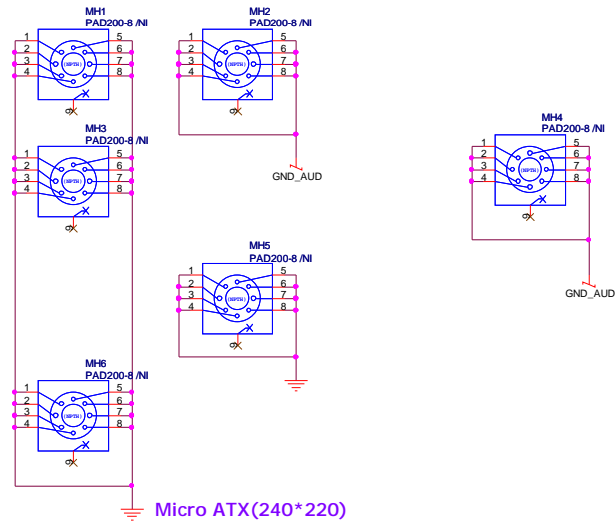






+1.5VDIMM_FB	VDIMM0	VDIMM1
Default 1.509V	1	1
1.547V	0	1
1.605V	1	0
1.644V	0	0

OVER VOLTAGE IC

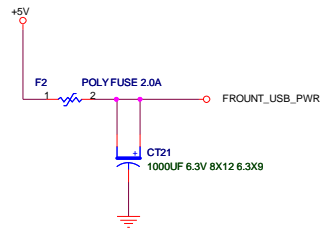


Micro ATX(240*220)

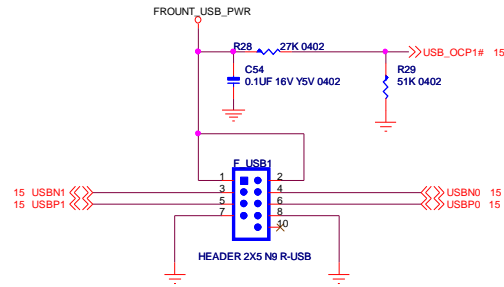
MT



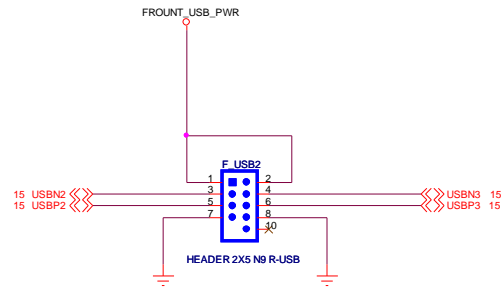
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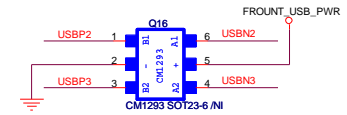
FRONT USB POWER



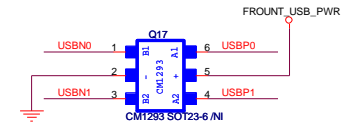
FRONT USB HEADER

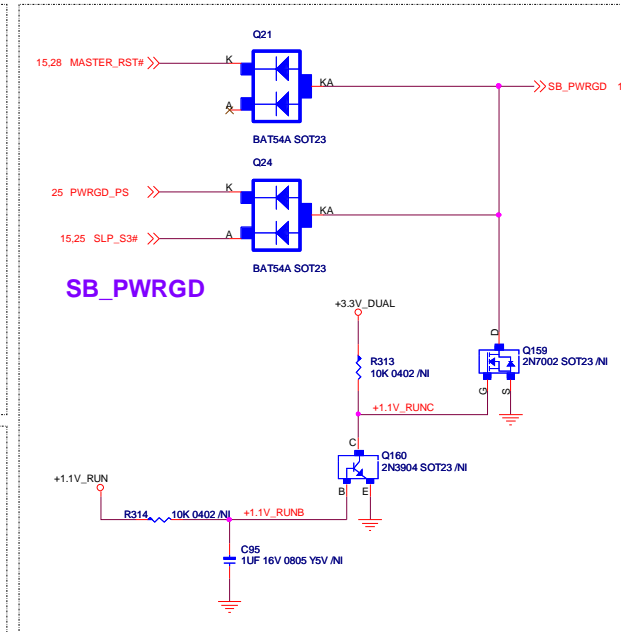
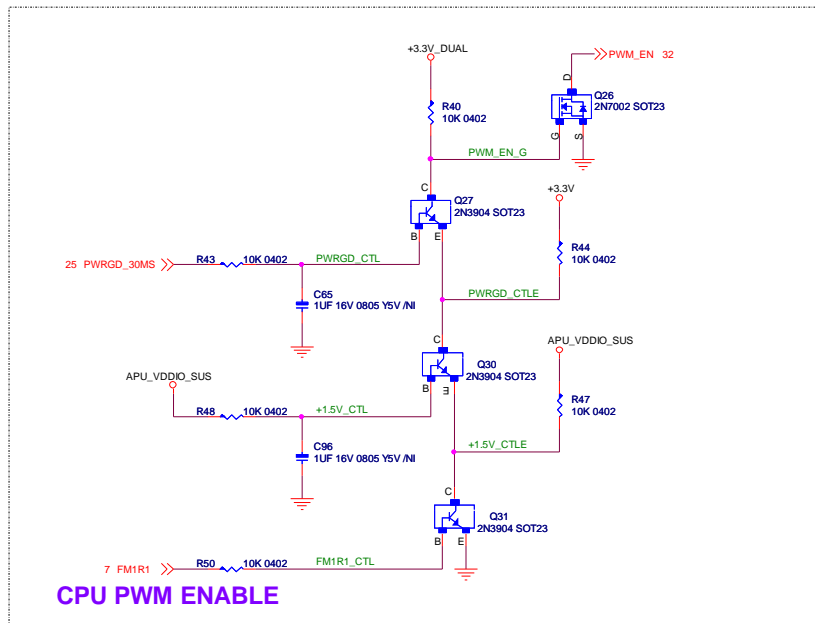
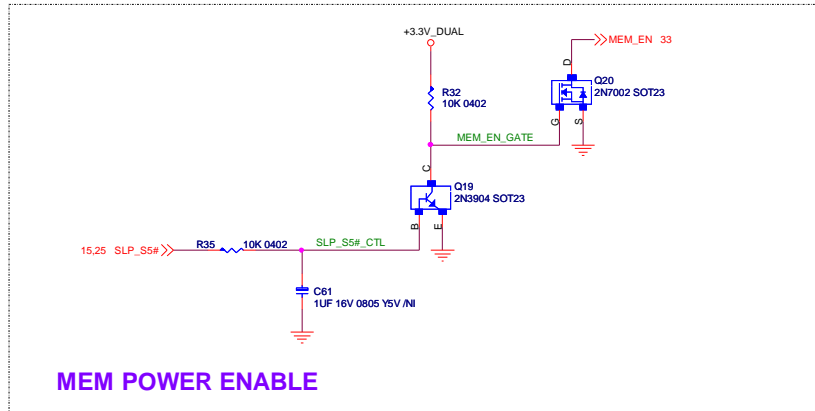


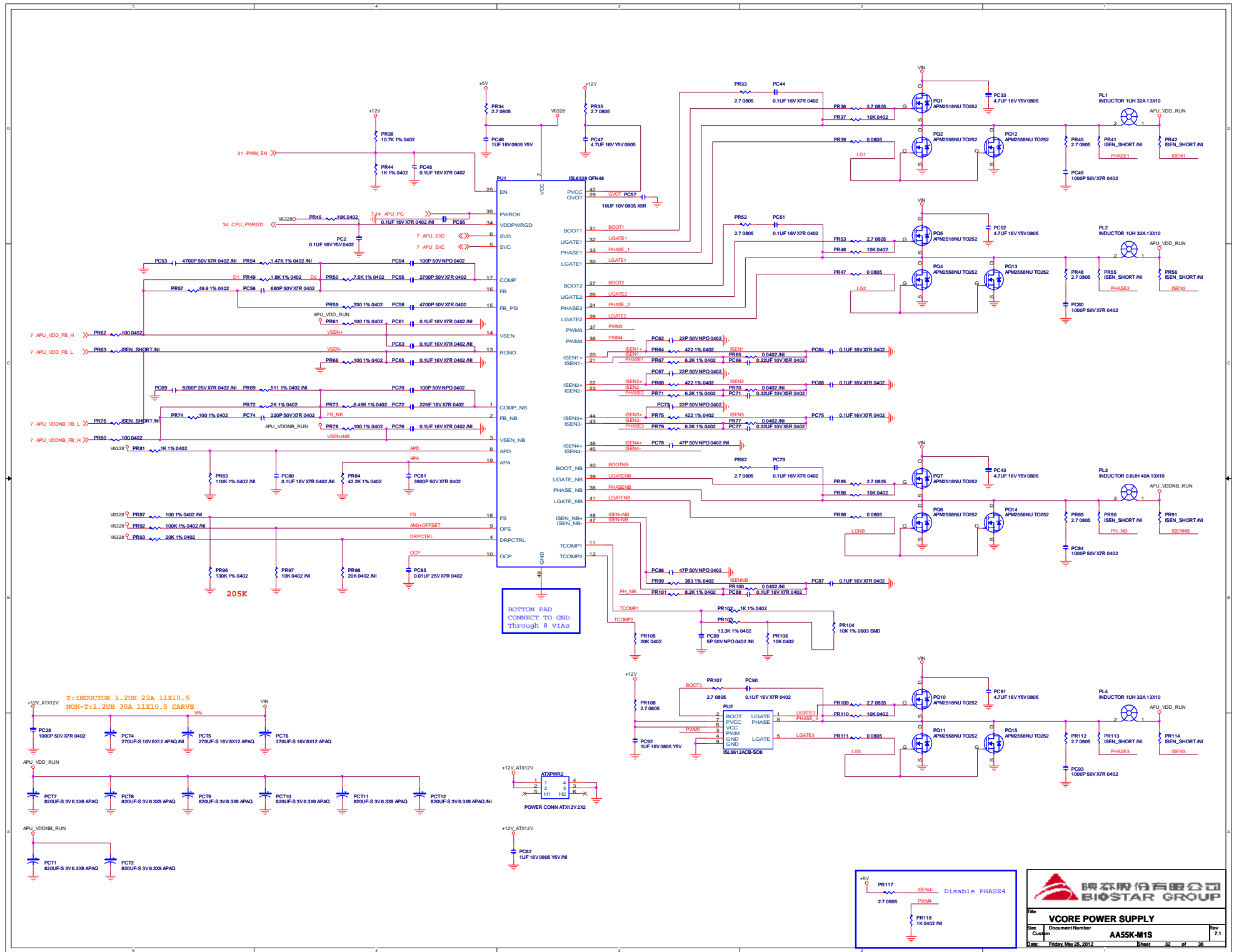
AMD Motherboard Design Guide 1.6 update

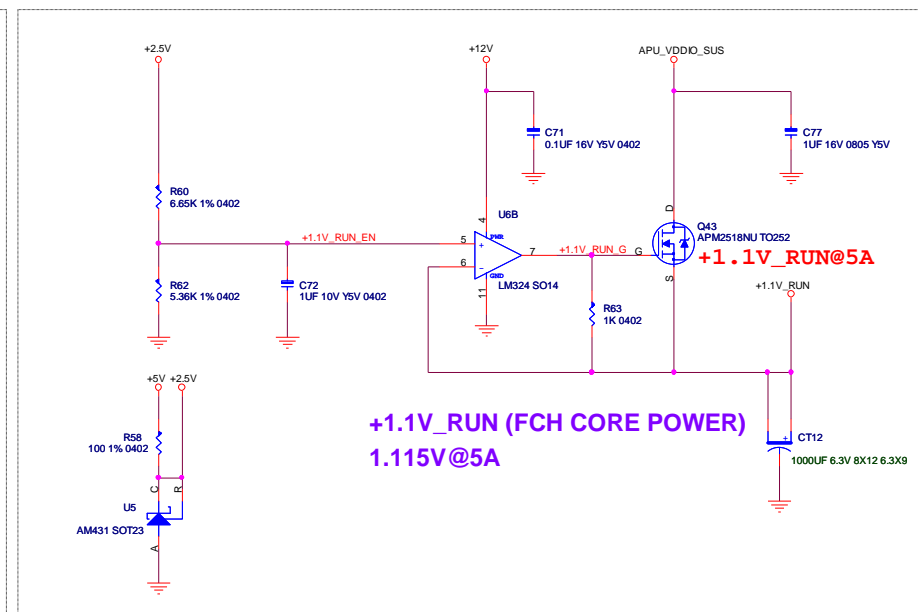
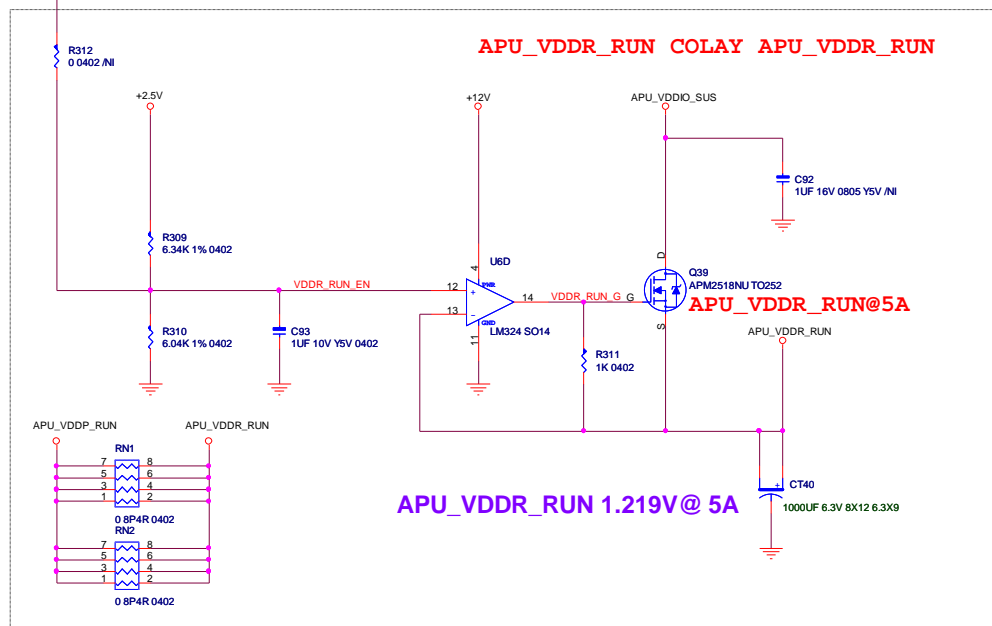
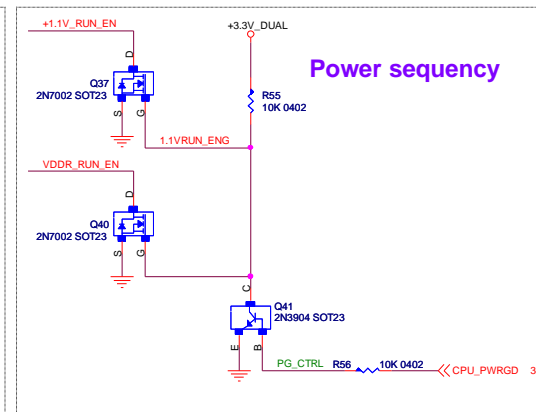
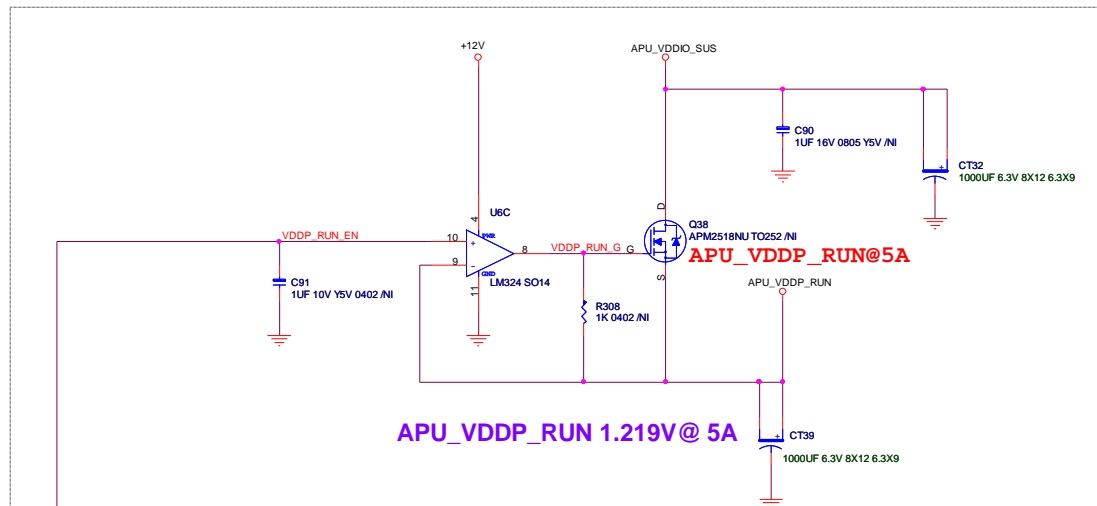


FRONT USB ESD









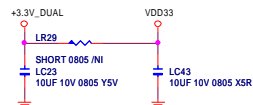
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4

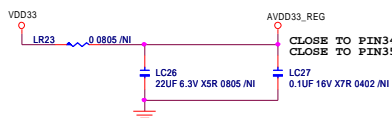
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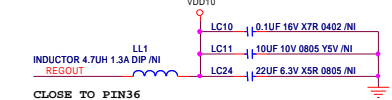
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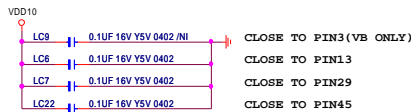
ENABLE SWITCHING REGULATOR : ADD
DISABLE SWITCHING REGULATOR : REMOVE



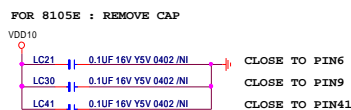
FOR 8111E/F : ADD



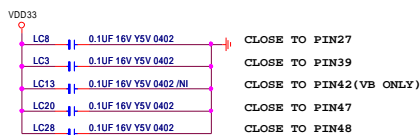
FOR 8105E : ADD CAP



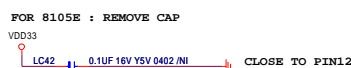
FOR 8111E/F : ADD CAP



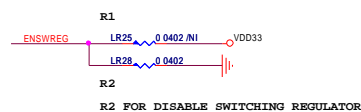
FOR 8105E : ADD CAP



FOR 8111E/F : ADD CAP



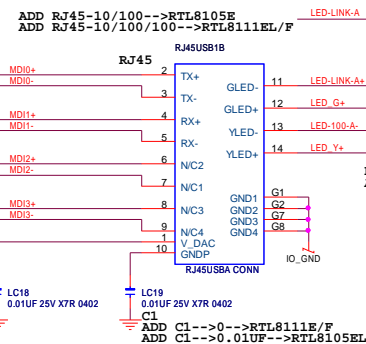
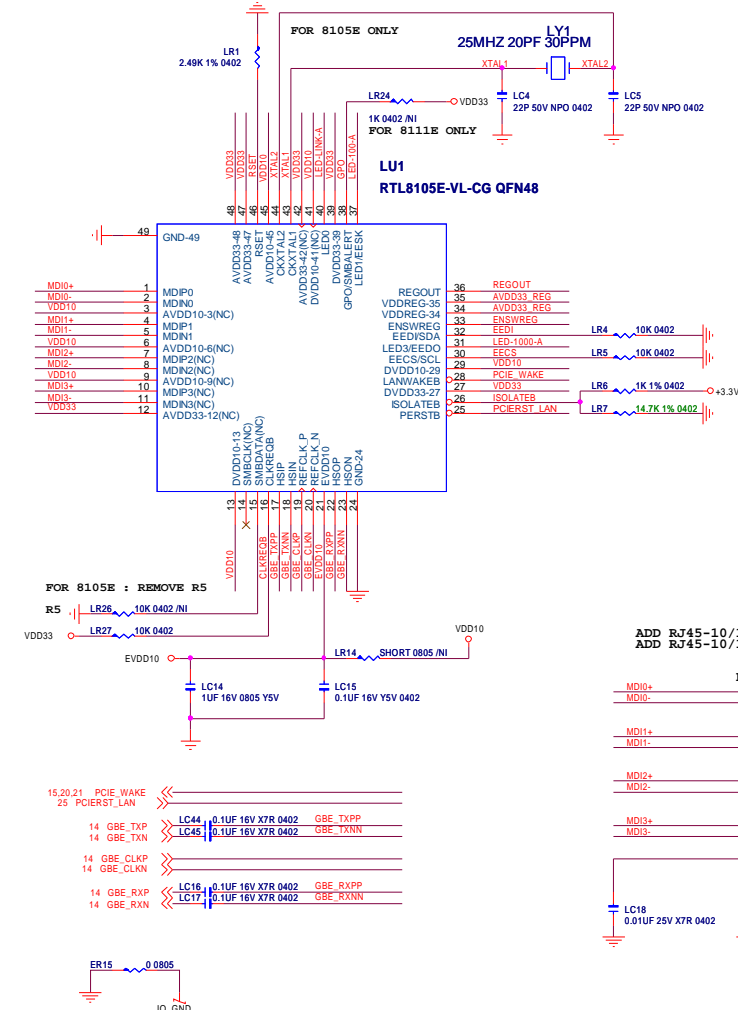
R1 FOR ENABLE SWITCHING REGULATOR



R2 FOR DISABLE SWITCHING REGULATOR

RTL8111E/8111F--> PIN(3,6,9,13,29,41,45):ADD 0.1UF CAP
RTL8105E-VB--> PIN(3,13,29,45):ADD 0.1UF CAP
RTL8105E--> PIN(13,29,45):ADD 0.1UF CAP

RTL8111E/8111F--> PIN(12,27,39,42,47,48):ADD 0.1UF CAP
RTL8105E-VB--> PIN(27,39,42,47,48):ADD 0.1UF CAP
RTL8105E--> PIN(27,39,47,48):ADD 0.1UF CAP



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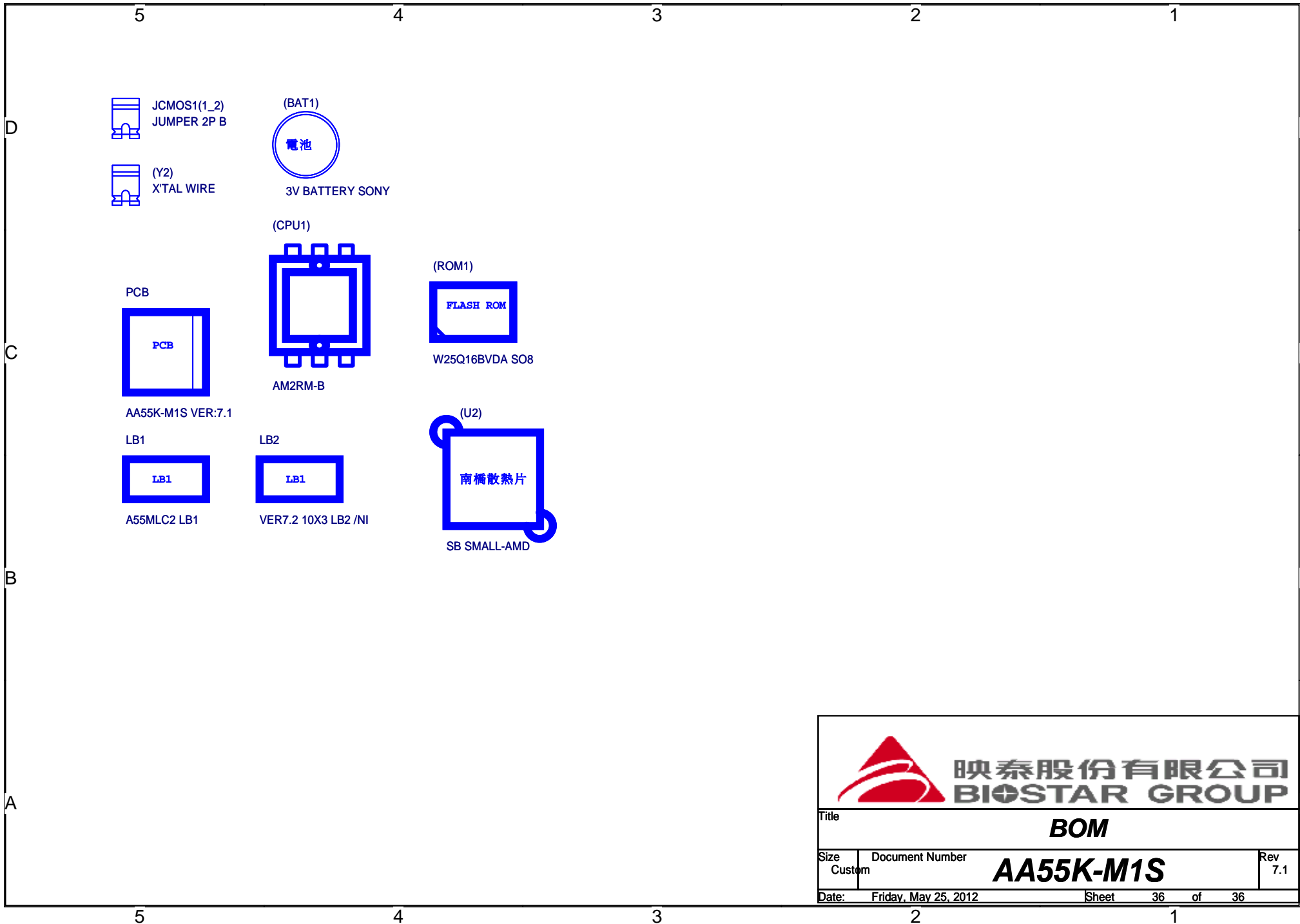
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4

3

2

1



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BOM			
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